IN THE CLAIMS

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

Claims 1 and 2. (Cancelled)

3. (Currently Amended) The wireless transceiver device ~~of claim 1~~ of claim 23 wherein the FIFO memory structure includes pointers that define addresses of the command blocks.

Claim 4. (Cancelled)

5. (Currently Amended) The wireless transceiver device ~~of claim 1~~ of claim 23, wherein the modulation circuitry includes Gaussian Phase Shift Keying modulation and the demodulation circuitry includes Gaussian Phase Shift Keying demodulation circuitry.

6. (Currently Amended) The wireless transceiver device ~~of claim 1~~ of claim 23 wherein ~~the frequency conversion circuitry~~ each of the up-converter and the down-converter converts directly between radio frequency and baseband frequency.

7. (Currently Amended) A method for storing and ~~transmitting data~~ accessing data in a baseband processing circuitry for transmission by a wireless communication device, comprising:

storing a data block in random access memory of the baseband processing circuitry; ~~and~~

storing a pointer that corresponds to the data block in a first in, first out (FIFO) memory structure of the baseband processing circuitry, the pointer includes an address of a command block;

storing an address of the data block in the command block; and

setting an indicator signal in a defined memory location, wherein the indicator signal indicates that the data block address stored in the command block is for data that has yet to be successfully transmitted by the wireless communication device and that the command block is busy.

Claims 8-10. (Cancelled)

11. (Currently Amended) The method of claim 7 wherein ~~an address for a data block~~ the address for the data block is only stored in a command block if the indicator signal reflects that the command block does not contain the address of a data block that has yet to be successfully transmitted.

12. (Previously Presented) The method of claim 7 further comprises:

evaluating the command block address included within the FIFO pointer.

13. (Currently Amended) The method of claim 12 further comprises:

examining the contents of the command block specified by the pointer to determine ~~a data block address~~ the data block address.

14. (Previously Presented) The method of claim 13 further comprises:

evaluating at least a first memory location of the data block whose address is stored in the command block to determine a data block size.

15. (Currently Amended) The method of claim 14 further comprises:

retrieving an amount of data corresponding to the data block size and ~~transmitting that data~~ providing the data to a radio modem for transmission over wireless airwaves.

16. (Currently Amended) The method of claim 15 further comprises:

resetting the indicator signal ~~if the transmission was successful~~ when the transmission is successful.

17. (Currently Amended) A memory structure formed within a ~~baseband processing system~~ baseband processing circuitry, comprising:

a random access memory portion defined within the baseband processing circuitry to store data blocks ~~for storing data blocks~~ that are to be transmitted via a radio modem in a first in, first out (FIFO) order; [[and]]

a FIFO memory structure defined within the baseband processing circuitry to store pointers ~~for storing pointers~~ that correspond to the data blocks stored in the random access memory portion;

a plurality of command blocks ~~defined within~~ further defined within the random access memory portion ~~wherein each command block is for specifying~~, wherein each of the command blocks specifies an address of a data block that is to be transmitted; and

a defined memory portion ~~for storing command block indicators~~ that stores command block indicators for each command block, wherein ~~the command block indicators~~ each of the command block indicators specify whether its corresponding command block includes the address of a data block that has yet to be ~~transmitted successfully~~ successfully transmitted via the radio modem.

Claims 18 and 19. (Cancelled)

20. (Currently Amended) The memory structure of claim 17 wherein ~~the defined memory portions for storing~~ the defined memory portion that stores the command block indicators are each one bit in length.

21. (Currently Amended) The memory structure of claim 17 wherein the command blocks ~~defined within~~ further defined within the random access memory portions are each four bytes in length.

22. (Currently Amended) The memory structure of claim 17 wherein the FIFO memory structure defines a plurality of FIFO memory blocks ~~wherein each FIFO memory block relates to~~ in which each FIFO memory block correspond to the data blocks that are to be transmitted to a particular device.

23. (New) A wireless transceiver device, comprising:

a transmit/receive switch to selectively transmit radio frequency signals and to receive radio frequency signals;

transmission circuitry to receive digital data and to convert the digital data to radio frequency signals for transmission, the transmission circuitry includes:

modulation circuitry coupled to receive the digital signals and produce modulated digital signals;

digital-to-analog conversion circuitry coupled to convert the modulated digital signals to converted analog signals;

up-converter coupled to receive to convert the modulated digital signals to produce outgoing radio frequency signals for transmission via the transmit/receive switch;

receiver circuitry coupled to receive radio frequency signals from the transmit/receive switch, the receiver circuitry includes:

down-converter coupled to receive the radio frequency signals from the transmit/receive switch and produce down-converted radio signals;

analog-to-digital conversion circuitry coupled to convert the down-converted radio signals to digital signals; and

demodulation circuitry coupled to receive the digital signals from the analog-to-digital conversion circuitry and produce demodulated digital signals; and

baseband processing circuitry coupled to provide the digital signals to the transmission circuitry and to receive the demodulated digital signals from the receiver circuitry, the baseband processing circuitry including:

a first in, first out (FIFO) memory structure for storing addresses for accessing data blocks to order the digital data to provide the transmitter circuitry; and

a plurality of command blocks formed within another memory structure, and a portion of the another memory structure that stores an indicator that indicates whether a command block of the plurality of command blocks is in use,

wherein each of the command blocks includes addresses of data blocks stored within the another memory structure.